Session 12 Overview

Nyquist ADCs

Chair: Venu Gopinathan, Texas Instruments, Bangalore, India

Associate Chair: Aaron Buchwald, Mobius Semiconductor, Irvine, CA

Analog-to-digital converters continue to play a vital role in virtually all applications ranging from sensor arrays to broadband communication. Power dissipation has always been important, but today is even more so with the emphasis on extended battery life for hand-held multi-media devices. Achieving both low-power dissipation and high resolution simultaneously requires excellent engineering, new circuit techniques, and architectural innovations.

The eight presentations in this session address challenges in ADC design in achieving resolutions of 10 to 14 bits over sample rates from DC to 100MS/s.

The first paper in this session discusses a 10-bit ADC with an energy per conversion-step of 0.5pJ in 90nm CMOS. In addition, this converter is designed to trade power for sampling rate from 25 to 100MS/s to obtain "speed-on-demand" with no sacrifice in energy efficiency.

The session continues with the next two papers highlighting various power-saving techniques. A method of opamp sharing by reusing opamp currents in different pipeline stages is presented in Paper 12.2. Next, simultaneous offset cancellation and positive-feedback gain boosting is discussed in Paper 12.3 that allows the use of smaller devices in comparators.

Paper 12.4 discusses a new method for switched-capacitor circuits using comparators instead of feedback-forcing opamps. A 10-bit 2.5mW 8MS/s ADC is designed in 0.18µm to demonstrate the concept.

The session takes a detour from the 100MS/s range to consider the challenge of achieving micro-watt power dissipation at 100kS/s for sensor applications. In Paper 12.5 an efficient successive-approximation 12-bit ADC is presented that achieves an effective number of bits of 10.5 while consuming only 25µW from a 1V supply.

The final three papers of this session highlight different aspects of achieving good linearity without excess power dissipation. Paper 12.6 discusses a 100MS/s multi-bit pipelined ADC in 0.13µm CMOS that uses calibration to obtain greater than 70dB THD and 66dB SNR while dissipating 224mW. Paper 12.6 is an implementation of a pipeline converter in 0.13µm CMOS that achieves an effective number of bits of 9.3 while consuming only 15mW and occupying an area of 0.2mm^2. Finally, a sorting algorithm to re-order capacitors in judicious groupings to minimize random mismatch is applied to the design of a 13-bit pipelined converter in 0.18µm CMOS.

12.1 A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step **8:30 AM**
G. Geelen, Philips, Eindhoven, The Netherlands

A 10b pipelined ADC with programmable speed and power achieves a power efficiency of 0.5pJ/conversion-step for sampling frequencies between 25 and 100MHz. Measurements show an ENOB of 9.3b, ERBW exceeding 100MHz, and THD<-65dB with a supply voltage of 1.2V. Chip area is 0.3mm^2 in a 90nm digital CMOS process.

12.2 A 10b 50MS/s Pipelined ADC with Opamp Current Reuse **9:00 AM**
S-T. Ryu, University of California, San Diego, La Jolla, CA

Power-saving techniques such as opamp current reuse and capacitive level shift reduce the power consumption of a 10b pipelined ADC to 220μW/MHz. A 50MS/s prototype in 0.18μm CMOS consumes 18mW (11mW for analog) at 1.8V and occupies 1.1×1.3mm^2. The measured ENOB of the ADC is 9.2b (8.8b) for a 1MHz (20MHz) input.

12.3 A 30mW 12b 40MS/s Subranging ADC with a High-Gain Offset-Canceling Positive-Feedback Amplifier in 90nm Digital CMOS **9:30 AM**
Y. Shimizu, Sony, Nagasaki, Japan

A 12b 40MS/s 2-step subranging ADC is realized in a 90nm digital CMOS process. It uses a 7b coarse quantizer with a high-gain offset-canceling positive-feedback amplifier. ENOB is 10.2b at a 0.7V supply and 11.0b at a 1.0V supply. The ADC consumes 30mW at 40MS/s.

12.4 Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies **10:15 AM**
T. Sepke, MIT, Cambridge, MA

A comparator-based switched-capacitor (CBSC) design method for sampled-data systems utilizes topologies similar to traditional opamp-based methods but relies on the detection of the virtual ground using a comparator instead of forcing it with feedback. A prototype 10b CBSC 1.5b/stage pipelined ADC is implemented in a 0.18μm CMOS process. The converter operates at 8MHz and consumes 2.5mW.

12.5 A 25μW 100kS/s 12b ADC for Wireless Micro-Sensor Applications **10:45 AM**
N. Verma, MIT, Cambridge, MA

A 0.18μm CMOS 12b 100kS/s successive approximation ADC is presented. The entire ADC consumes 25μW from a 1V supply and achieves an SNDR of 65dB. Its sampling rate can be scaled, yielding linear power savings. Efficiency of the comparator is increased by an offset compensating latch, while noise performance and common-mode rejection are improved by a modified capacitor network.

12.6 A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13μm CMOS **11:15 AM**
P. Bogner, Infineon, Villach, Austria

A 14b multi-bit-per-stage pipelined ADC is implemented in a 0.13μm digital CMOS process. The gain and matching errors of the analog circuitry are compensated by a digital calibration scheme that allows the usage of a low-gain op-amp. A low power consumption has been reached by introducing a charge compensation scheme.

12.7 A 15mW 0.2mm^2 10b 50MS/s ADC with Wide Input Range **11:45 AM**
H-C. Choi, Samsung, Yongin-City, Korea

A 10b 50MS/s pipelined ADC, implemented in a 0.13μm CMOS process, consumes of 15mW and occupies an active die area of 0.2mm^2. In the prototype ADC, a high-to-low analog level-shifting SHA is proposed to deal with a wide input range of $2V_{pp}$ differential. A PVT-insensitive bias generator is employed for low voltage operation. The measured DNL and INL are ±0.17LSB and ±0.16LSB, respectively.

12.8 A 13b Linear 40MS/s Pipelined ADC with Self-Configured Capacitor Matching **12:00 PM**
S. Ray, University of California, San Diego, CA

Using statistical matching properties of capacitor arrays, a pipelined ADC self-configures the MDAC capacitor array for best matching from many trial combinations. A 0.18μm CMOS prototype achieves 13b linearity and over 80dB SFDR at 43MS/s. The chip consumes 268mW from a 1.8V supply and occupies 3.6mm^2.